REMARKS

Claims 1-8 are pending in the application. No amendment is made to the description or drawings. No new matter is added.

Claim Rejections - 35 *USC* § 112

Claims 1-8 stand rejected under 35 USC §112, second paragraph as being indefinite. Applicant respectfully traverses the rejection.

Regarding claim 1

The Office Action states that "Regarding claim 1, the recitation "said continuous-time sigma-delta modulator being connected to said combiner to utilize said train of combined return-to-zero clock pulses as clock" is confusing" and states that "The "train of combined return-to-zero clock" is signal (CLK_JF) is not seen to connected to the "continuous-time sigma-delta modulator"."

Applicant respectfully traverses this rejection. Applicant submits that the recitations of claim 1 referred to are clear and are not confusing and that the description in the specification of embodiments of the invention contains a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, as required by 35 USC §112.

The "clock pulse generator apparatus" and its clock pulse output are connected to the "continuous-time sigma-delta modulator"

Page 3 lines 16-22 of the specification states:

"Figure 1 is a block schematic diagram of a continuous-time Analogue-to-Digital sigma-delta modulator to which the present invention may be applied,

Figure 2 is a block schematic diagram of a continuous-time Digital-to-Analogue sigma-delta modulator to which the present invention may be applied" and

"Figure 5 is a block schematic diagram of a clock pulse generator in accordance with one embodiment of the invention".

Page 7 lines 9-11 states: "Unlike the prior art techniques, this embodiment of the present invention" (shown in Figure 5) "avoids interfering with the normal operation of the circuit" (of Figure 1 or 2) " but rather focuses on attenuating jitter within the clock signal before it is applied to the circuit." (of Figure 1 or 2).

Applicant submits that these passages clearly indicate that the clock pulse generator apparatus of Figure 5 and its clock pulse output (CLK_JF) are connected to the "continuous-time sigma-delta modulator" (of Figure 1 or Figure 2) as recited in claim 1.

The continuous-time sigma-delta modulator is connected to the combiner to utilize said train of combined return-to-zero clock pulses as clock

The output (CLK_JF) of the clock generator of Figure 5 (which is applied to the circuit of Figure 1 or 2) is stated at page 7 lines 21-28 to be "As depicted in Figure 3, RTZ signal has an active clock phase ('ACP') and a non-active clock phase ('NACP')... This embodiment of the present invention makes the width of the ACP relatively jitter-free while allowing most of the jitter to be absorbed by the NACP. ... This is achieved with a clock generator ... as shown in Figure 5."

Page 7 line 32 to page 8 line 3 states "Both the clock and the delayed clock (CLK_D) signals are applied as inputs to the logic AND/NAND circuit 15, whose output CLK_JF is asserted at the leading edge of the CLK signals and is de-asserted at the leading edge of the CLK_D signals."

The clock signal is applied to the continuous-time sigma-delta modulator circuit of Figure 1 or 2. (page 7 lines 9-11)

Applicant submits that these passages clearly indicate that the logic circuit 15, the combiner, produces a "train of combined return-to-zero clock pulses" (the output (CLK_JF) of the clock generator of Figure 5) which is utilized by the continuous-time sigma-delta modulator.

Applicant submits that these passages clearly support the recitation in claim 1 of "said continuous-time sigma-delta modulator being connected to said combiner to utilize said train of return-to-zero clock pulses as clock".

Regarding claim 6

The Office Action states that "The same rationale is applied to the recitation "wherein said continuous-time sigma-delta modulator comprises a digital-to-analogue converter module whose operation is responsive to said train of return-to-zero clock pulses" in claim 6.

As Applicant submits above, the passages quoted clearly indicate that the clock pulse generator apparatus of Figure 5 and its clock pulse output (CLK_JF) are connected to the "continuous-time sigma-delta modulator" of Figure 1 or Figure 2. Specifically, both the modulators of Figure 1 and Figure 2 include digital-to-analogue converter modules ('DAC's 5 & 9) responsive to the clock signal (CLK).

As stated at page 7 lines 9-11 "Unlike the prior art techniques, this embodiment of the present invention" (shown in Figure 5) "focuses on attenuating jitter within the clock signal before it is applied to the circuit." (of Figure 1 or 2).

Applicant submits that these passages clearly indicate that the clock pulses to which the DACs 5 & 9 of Figures 1 & 2 are responsive are the train of combined return-to-zero clock pulses of the clock pulse output (CLK_JF) of the generator apparatus of Figure 5, as recited in claim 6 with reference to the antecedent in claim 1.

***Claim Rejections* - 35 *USC* § 102**

Claims 1 and 2 are rejected under 35 U.S.C. 102 (b) as being anticipated by Kim et al. (US 6,307,412).

Claim 1 recites "a combiner for producing said train of return-to-zero clock pulses presenting leading and trailing edges defined alternately by one of said delayed edges and said corresponding edges of said first clock pulses, so that the active clock phases of said return-to-zero clock pulses have widths defined by said delay module". Applicant respectfully submits that Kim et al does not disclose a combiner producing a train of pulses presenting leading and trailing edges defined alternately by one of said delayed edges and said corresponding edges of said first clock pulses, as required by claim 1.

Applicant also submits that Kim et al does not disclose a train of pulses whose active clock phases of said return-to-zero clock pulses have widths defined by said delay module, as also required by claim 1.

Applicant also submits that Kim et al does not disclose a train of pulses in which the variability of said widths of said active clock phases is smaller than the variability of the positions of said leading and trailing edges of said first clock pulses, as also required by claim 1.

Leading and trailing edges defined alternately by one of said delayed edges and said corresponding edges of said first clock pulses

The Office Action states that Kim et al discloses the feature of "a train of clock pulses (CK) presenting leading and trailing edges defined alternately by one of said delayed edges and said corresponding edges of said first clock pulses (XCK)" as recited in claim 1. However, Applicant submits that the train of clock pulses (CK) of Kim et al presents leading edges defined by the leading edges of the 'first' clock pulses (XCK) and trailing edges defined by the trailing edges of the delayed pulses (DXCK). The leading and trailing edges of the train of clock pulses from the combiner of Kim et al are not defined alternately by one of said delayed edges and said corresponding edges of said first clock pulses, as recited in claim 1.

For Kim et al to teach this feature recited in claim 1, since the train of clock pulses (CK) of Kim et al present leading edges defined by the leading edges of the 'first' clock pulses (XCK), the trailing edges of clock pulses (CK) would have had to be defined by the leading edges of the delayed pulses (DXCK), which is not the case: see Fig. 4 of Kim et al, arrows from the leading edges of XCK to the leading edges of CK, and arrows from the trailing edges of DXCK to the trailing edges of CK. Alternatively, for Kim et al to teach the above feature recited in claim 1, since the train of clock pulses (CK) of Kim et al presents trailing edges defined by the trailing edges of the delayed pulses (DXCK), the leading edges of clock pulses (CK) would have had to be defined by the trailing edges of the 'first' clock pulses (XCK), which is not the case.

Accordingly, Applicant submits that Kim et al does not disclose a combiner for producing a train of pulses presenting leading and trailing edges defined alternately by one of said delayed edges and said corresponding edges of said first clock pulses, as required by claim 1. Applicant submits that accordingly Kim et al does not anticipate claim 1.

Widths defined by said delay module

The Office Action states that Kim et al discloses the feature of "a train of pulses whose active clock phases of said return-to-zero clock pulses have widths defined by said delay module", as recited in claim 1. However, Applicant submits that the width of the high state of the train of clock pulses (CK) of Kim et al is equal to the sum of the delay t1 and the width t2 of the

delayed clock pulses (DXCK) – see Fig. 4 of Kim et al. (Conversely, the width of the low state of the train of clock pulses (CK) of Kim et al is equal to the difference between the width t2 of the delayed clock pulses (DXCK) and the delay t1). Applicant submits that accordingly the active clock phases in Kim et al do not have widths defined by the delay module, as recited in claim 1 but are defined by the sum of delay t1 of the delay module and the width t2 of the delayed clock pulses (DXCK). Applicant submits that accordingly Kim et al does not anticipate claim 1.

Variability of the widths of the active clock phases

The Office Action states that Kim et al discloses the feature of "the variability of said widths of said active clock phases being smaller than the variability of the positions of said leading and trailing edges of said-first clock pulses", as recited in claim 1. However, the pulse widths of Kim et al are equal to the sum (or difference) of the delay t1 and the width t2 of the delayed clock pulses (DXCK). Applicant submits that therefore the variability of the widths of the active clock phases of Kim et al is equal to the variability of the width t2 of the delayed clock pulses (DXCK) plus any variability of the delay t1 and is therefore as great or greater than the variability of the positions of the leading and trailing edges of the first clock pulses (XCK = DXCK). Applicant submits that accordingly Kim et al does not anticipate claim 1.

Claim 2 depends from claim 1 and contains all the limitations thereof. Applicant submits that, at least for this reason, Kim et al does not anticipate claim 2.

Regarding claims 3, 4, 5-8

Claims 3, 4, 5-8 are indicated to be allowable if the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action are overcome. Appreciation is expressed for the allowance of these claims.

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action since reasons for the patentability of each pending claim are provided without addressing these statements. Therefore, Applicants reserve the right to address these statements at a later time if necessary.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the

scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

Respectfully submitted,

SEND CORRESPONDENCE TO:

By: /David G. Dolezal/

Freescale Semiconductor, Inc.
Law Department
Customer Number: 23125

David G. Dolezal
Reg. No.: 41,711
Telephone: (512) 996-6839
Fax No.: (512) 996-6854